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Claims 15-18 are in the Application. Independent claim 15 has been rejected as being anticipated in Suga et al. U.S. Patent 5,132,803. Applicant respectfully traverses this rejection and requests reconsideration.

In the prior Amendment, Applicant added the single word "solely" to the recitation describing each color register of the independent claim, in order to remove rejection by the Examiner based on Kawahara et al. in view of Uchiyama et al., even though the Examiner had apparently recognized, earlier on, that patentable subject matter was probably present over these citations, if Applicant could devise claim language satisfactory to the Examiner.

Now, after withdrawing the previous rejection based on Kawahara et al. and Uchiyama et al. (which had followed an earlier anticipation rejection based on Yamada et al., which was also previously withdrawn), and dealing with essentially the same invention, the Examiner has found a new citation, Suga et al., applied it in a rejection of the independent claim 15, and made the rejection "final." This may be technically within the Rules (since Applicant previously made the small amendments to claim 15 noted above), but is certainly harsh in light of the overall prosecution circumstances regarding the subject invention. Applicant respectfully requests open minded reconsideration of the new rejection, even under the existing "final" status.

Claim 15 recites an apparatus for producing electronic video signals

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representative of color images of a scene, including: a sensor having a color filter thereover; a lens system that focuses light from the image onto the color filter and sensor; and means for producing electronic video signals from the output of the sensor; the sensor comprising a sensor array having alternate lines offset by half a pixel spacing, and diagonally coupled pixels on successive lines, and the color filter having repeating R, G, and B patterns offset on successive lines so that R pixels are arranged diagonally, G pixels are arranged diagonally, and B pixels are arranged diagonally, the means for producing electronic video signals from the output of the sensor including a first register to which are connected R pixels, diagonally offset in alternating directions, for successive vertically adjacent lines of a group of lines, a second register to which are connected G pixels, diagonally offset in alternating directions, for successive vertically adjacent lines of the group of lines, and a third register to which are connected B pixels, diagonally offset in alternating directions, for successive vertically adjacent lines of the group of lines.

Suga et al. U.S. Patent 5,132,803 discloses an image pickup device having a plurality of photo-electric conversion elements disposed in plural rows, the elements being staggered by a half pitch from row to row. A memory stores a signal charge for at least one field from said image pickup line by line. The signals stored in the memory unit are then read out of the memory and input into three read-out units. In the Suga et al. invention, two neighboring rows of the memory unit at a time are read out alternately and divided between the three read-out units.

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In rejecting claim 15, the Examiner refers to the block diagram of Figure 8 of Suga et al. as including some of the elements of the claims at issue, and then Figure 16 of Suga et al. as including most of the key elements. The Examiner's correlations to the claim language of independent claim 15 include the following:

"....the sensor comprising a sensor array having alternate lines offset by half a pixel space, and diagonally coupled pixels on successive lines, and the color filter having repeating R, G and B patterns offset on successive lines so that R pixels are arranged diagonally, G pixels are arranged diagonally and B pixels are arranged diagonally (Figure 16, R, G and B pixels 10C); the means for producing electronic video signals from the output of the sensor including a first register to which are connected solely R pixels, diagonally offset in alternating directions, for successive lines of a group of lines (Figure 16, Item 20R), a second register to which are connected solely G pixels, diagonally offset in alternating directions, for successive lines of a group of lines (Figure 16, Item 20G) and a third register to which are connected solely B pixels, diagonally offset in alternating directions, for successive lines of a group of lines (Figure 16, Item 20B)."

However, an analysis of Suga et al. reveals that the citation does not operate as indicated in the above-quoted paragraph, and certainly does not anticipate the claimed invention. Specifically, the registers 20 of Suga et al. Figure 16 can be seen to be performing a timing function. The register taps are coupled to respective gates of field-effect devices (23), operating to switch these field-effect devices on or off, depending on the status of the register signals. The relevant Suga et al. Patent text (at Column 11) has sparse description of this part of Figure 16, but reference can be made to similar circuitry in Figure 10 and the description at Col. 9, which reads:

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"For reading the photoelectrically converted signals of respective colors, there are provided three circuits. Output signal lines 18R, 18G, 18B are for respectively reading signals of R, G, B stored in the designated rows of the frame memory 15. There are further provided horizontal readout shift registers 20R, 20G, 20B for designating the signals to be read from the frame memory 15; switches 23 controlled by the outputs of said shift registers 20R, 20G, 20B; output buffers 24R, 24G, 24B; and output terminals 26R, 26G, 26B. The shift registers 20R, 20G, 20B are activated by a start pulse STATH, and receive shift pulses  $\Phi_{SA}$ ,  $\Phi_{SB}$ ,  $\Phi_{SC}$ .

"There are also provided an address decoder 29 for simultaneously activating two adjacent ones of the vertical address lines 10V of the photoelectric conversion unit 10; and a decoder drive circuit 31 for designated (sic) the vertical address lines to be activated by the address decoder 29, according to the vertical address data  $D_{VA}$ . Said vertical address data  $D_{VA}$  are for example of 9 bits of which the first bits indicate an odd field or an even field, and the remaining 8 bits designate the vertical address. The address decoder 29, as will be explained later in detail, sends a readout clock signal  $\Phi_H$  to two vertical address lines 10V determined by the above-mentioned vertical address and the odd/even signal from the decoder drive circuit 30, and sends a clock signal  $\Phi_L$  to other vertical address lines. Thus the readout clock signal is supplied simultaneously to two vertical address lines 10V, for example to the first and second rows or third and fourth rows in case of an odd field, or to the second and third rows or the fourth and fifth rows in case of an even field."

Thus, it is evident that the Examiner's above-quoted argument that, for example, Figure 16, item 20R corresponds to "means for producing electronic video signals from the output of the sensor including a first register to which are connected solely R pixels,

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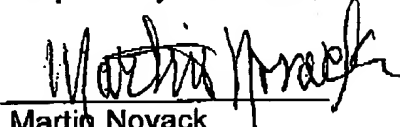
diagonally offset in alternating directions, for successive lines of a group of lines" is completely misplaced. Contrast, for example, Applicant's Figure 5, in which the horizontal register for red is receiving R pixels, diagonally offset in alternating directions, for successively vertically adjacent lines of a group of lines, and the same is true for the blue and green registers. As seen from the foregoing, the frame memory of Suga et al. is doing something different and does not operate this way. Accordingly, the rejections of independent claim 15, and the claims which depend therefrom, should be vacated.

In view of the foregoing, it is believed that the Application is now in condition for allowance, and such favorable action is earnestly solicited. In the event that the Examiner is not persuaded, it is asked that he kindly telephone the undersigned Counsel collect so that any remaining issues can be resolved.

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November 29, 2006

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